APPENDIX I- CLAIMS

1. An asynchronously-accessible storage device comprising:

mode circuitry configured to select between a burst mode and a pipelined mode; and

circuitry operable in either a burst mode or a pipelined mode coupled to the mode selection circuitry and configured to switch between the pipelined mode and the burst mode for operating the asynchronously-accessible storage device in either mode.

2. The asynchronously-accessible storage device of Claim 1 wherein the burst mode and the pipelined mode are extended data out modes of operation.

3. The asynchronously-accessible storage device of Claim 1 wherein the pipelined mode is an extended data out mode.

4. The asynchronously-accessible storage device of Claim 1 wherein the burst mode is an extended data out mode.

5. The asynchronously-accessible storage device of Claim 1 wherein the piplined/burst mode circuitry includes a buffer, the buffer for storing an address.

6. The asynchronously-accessible storage device of Claim 5 wherein the piplined/burst mode circuitry includes at least one counter for incrementing the address.

7. The asynchronously-accessible storage device of Claim 1 wherein the pipelined/burst mode circuitry is coupled for reading an external address.

8. The asynchronously-accessible storage device of Claim 7 wherein the pipelined/burst mode circuitry includes a buffer for storing the external address.

9. The asynchronously-accessible storage device of Claim 7 wherein the pipelined/burst mode circuitry includes mutliplexed devices for providing an internally generated address to the storage device.

33. A method for accessing a storage device, comprising:

receiving a first address to the storage device;

selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode of operation of the storage device;

selecting between outputting information from the storage device and inputting information to the storage device;

obtaining a second address to the storage device; and

asynchronously accessing a storage element of the storage device in the selected mode of operation using the first address and the second address.

34. The method of Claim 33, further comprising switching between the burst mode and the pipelined mode.

35. The method of Claim 33, wherein the second address is an external address.

46. A method for accessing several different locations in an asynchronously-accessible memory device, comprising:

selecting a pipelined mode of operation;

providing a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in the pipelined

mode of operation;

switching modes to a burst mode of operation;

providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the burst mode of operation; and

generating at least one subsequent internal address patterned after the initial external address while in the burst mode of operation.

48. The method of Claim 46 wherein the burst mode operates in an environment selected from the group consisting of column-based switching, row-based switching, application based switching, and fixed access-based switching.

49. The method of Claim 46 wherein the pipelined mode operates in an environment selected from the group consisting of column-based switching, row-based switching, application based switching, and fixed access-based switching.

50. A system comprising:

a microprocessor;

a memory, coupled to the microprocessor, the memory selectively operable either in a burst mode or a pipelined mode, wherein the memory is an asynchronous dynamic random access memory; and

a system clock coupled to the microprocessor.

59. A method for accessing a storage device, comprising:

receiving a first address to the storage device;

receiving a burst/pipeline signal;

selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode of operation of the storage device in response to the burst/pipeline

signal;

obtaining a second address to the storage device; and

accessing a storage element of the storage device in the selected mode of operation using the first address and the second address.

60. A method for accessing a storage device, comprising:

receiving a first address to the storage device;

receiving a burst/pipeline signal;

selecting between outputting information from the storage device and inputting information to the storage device;

selecting between an asynchronously-accessible burst mode and an asynchronously-accessible pipelined mode of operation of the storage device in response to the burst/pipeline signal;

obtaining a second address to the storage device; and

asynchronously accessing a storage element of the storage device in the selected mode of operation using the first address and the second address.

61. A method for accessing several different locations in an asynchronously-accessible memory device, comprising:

selecting a pipeline mode of operation;

providing a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in a burst mode of operation;

switching modes to the burst mode of operation;

providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the pipelined mode of operation; and

while in the burst mode of operation, generating at least one subsequent internal address patterned after the initial external address provided while in the pipelined mode of operation.

63. A storage device, comprising:

an array of memory cells;

mode circuitry for receiving a burst/pipeline signal; and

operation circuitry operable in a burst or a pipeline mode of operation depending upon the burst/pipeline signal, the operation circuitry switchable between burst and pipeline modes of operation.

64. A memory circuit, comprising:

an array of memory cells;

burst/pipeline selection circuitry for determining a burst or a pipeline mode of operation of the memory circuit; and

mode circuitry capable of operation in either a burst mode or a pipeline mode of operation, and switchable between burst and pipeline modes of operation.

Company

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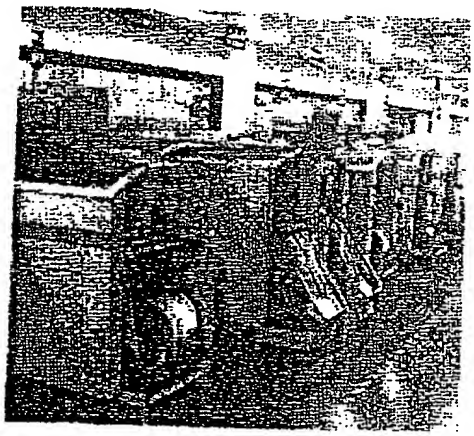

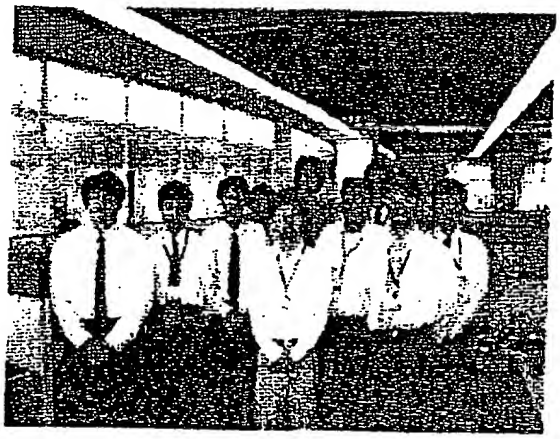

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The Research and Development engineers highly experienced and creative. For 1! professionals are always in pursuit of i maintaining product's price per performance quality. Fully equipped with hi-end CAD too intensive research of up-to-date technology, professionals at SHUTTLE have provided super have been proven in the market for over a dec

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Our company is a member of the global together with the whole global enterprises t the green environment. We are dedicated protection of the environment and the environmental pollution, for the minimizing o handling of energy conservation, as well as to related legal requirements. This is to allow th be able to have our manufactured green p eventually protect our environment.

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- Re-use the recyclable resources
- Conserve energy which shall be done by everyone
- Aspire for green products

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SHUTTLE strongly believes in teamwork partnership with customers and remains firmly committed to delivering products with the highest quality, optimum performance and value.

SHUTTLE Contact List

Asia

America

Germany

Company

Taiwan Head Quarters:
Shuttle INC.
NO. 30, Lane 76, Rei Kuang Rd.
Nei-Hu Dist., Taipei, Taiwan
TEL: 886-2-8792-6168
FAX: 886-2-8792-6268

US Sales Office:
Shuttle Computer Group INC.
939 Radecki Court City of Industry, CA
91748, U.S.A.
TEL: 626-820-9000
FAX: 626-820-5060
http://www.shuttleonline.com

Germany Sales Office:
Shuttle Computer Handels G
Fritz-Strassmann Str. 5
D-25337 Elmshorn, Germany
TEL: 49-4121-476860
FAX: 49-4121-476900

Frequently Asked Questions

SIMMs and DIMMs

Chapter set below:
SIMMs (Single In Line Memory Modules)
DIMMs (Dual In Line Memory Modules)

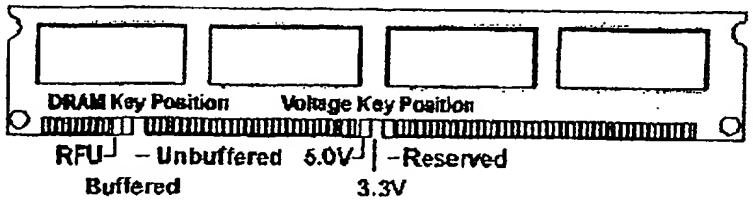
The names SIMM and DIMM only specifies the package RAM comes in, not the type! You can get each RAM type (FPM, EDO, SDRAM,...) for each module, but as fas as PCs are concerned, DIMMs are at present only used for SDRAM.

SIMMs (Single In Line Memory Modules)

SIMMs have 72 Pins and data path width of 32 Bit (36 Bit using Parity-Modules). On Pentium-Mainboards two SIMMs of the same kind and capacity have to be used to fill a bank. Some chipsets (for exp. SIS) allow to use only one module which results in a high performance loss.

DIMMs (Dual In Line Memory Modules)

DIMMs have 168 Pins. The data path width is 64 Bit (72 Bit using Parity-Modules). For this reason you can use a single DIMM to fill a bank on a Pentium-Board. Modules must be 3.3V Unbuffered SDRAM or EDO (you can identify type as shown by the illustration above).



Types of memory (FPM, EDO, SDRAM, ...)

Chapter set below:
Fast Page Mode (FPM)
Extended Data Output RAM (EDO)
Burst Extended Data Output RAM (BEDO)
Synchronous Dynamic RAM (SDRAM)

Fast Page Mode (FPM)

Fast Page Mode are standard memory modules. Actually VRAM or Video RAM is nothing much different, it only is so called dual ported, which means it can be accessed by the

RAMDAC independently of the CPU accesses via the second port, so that the RAMDAC doesn't have to wait for the CPU access to finish. FPM DRAMs for mainboards comes in two different flavors nowadays: 60ns and 70ns access time. On 66 MHz system-clock you should use 60ns modules, however, 70ns work in most cases as well. "Fast Page Mode" means that the module assumes that the next access is in the same memory area (ROW) to speed up the operation. The fastest access in CPU-Cycles is 5-3-3-3 for a data burst of 4 (Byte / Word / Dword).

Extended Data Output RAM (EDO)

The major difference between FPM and EDO is the timing of the CAS#-Signal and Data output using a latch. This speeds up sequential read-operations. The fastest access in CPU-Cycles is 5-2-2-2.

Burst Extended Data Output RAM (BEDO)

In opposition to EDO data latch on BEDO is replaced by a register (i.e. an additional latch stage is added) data will not reach the outputs as a result of the first CAS cycle. The benefit of this internal pipeline stage is that data will appear in a shorter time from the activating CAS edge in the second cycle (i.e. tcas is shorter). The second difference is that BEDO devices include an internal address counter so that only the initial address in a burst of four needs to be provided externally. The fastest access in CPU-Cycles is 5-1-1-1.

Synchronous Dynamic RAM (SDRAM)

As the name says already, this RAM is able to handle all input and output signals synchronized to the system clock - that is something a short while ago only Static Cache RAM was able to achieve. System clock can be higher than 66Mhz. „PC/100"-modules support 100 MHz clock frequency for chipsets with this feature (e.g. Intel 440BX or VIA MVP3). The fastest access in CPU-Cycles is 5-1-1-1 (as fast as BEDO).

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